

GENERAL DESCRIPTION

The ft2012 is a high efficiency stereo, filterless, Class-D audio power amplifier. The ft2012 can operate from 2.7V to 5.5V supply. When powered with 5V voltage, the ft2012 can deliver 2.8W/channel (with 4Ω load) or 1.65W/channel (with 8Ω load). When packaged in WCSP, the output power of the ft2012 will be thermally limited to a lower value.

As a Class-D audio amplifier, the ft2012 features 90% efficiency and 75dB PSRR at 217Hz which make the device ideal for use in battery-supplied portable electronic devices. The ft2012 also features independent shutdown control for each channel. The gain can be selected to 6, 12, 18, or 24dB utilizing the G0 and G1 gain-select pins. Furthermore, the ft2012 minimizes click and pop noise during the turn-on and shutdown.

The ft2012 is available in WCSP-16 and QFN4X4-20 packages.

APPLICATIONS

- Mobile phone
- Portable digital assistant (PDA)
- Mini sound box

APPLICATION CIRCUIT

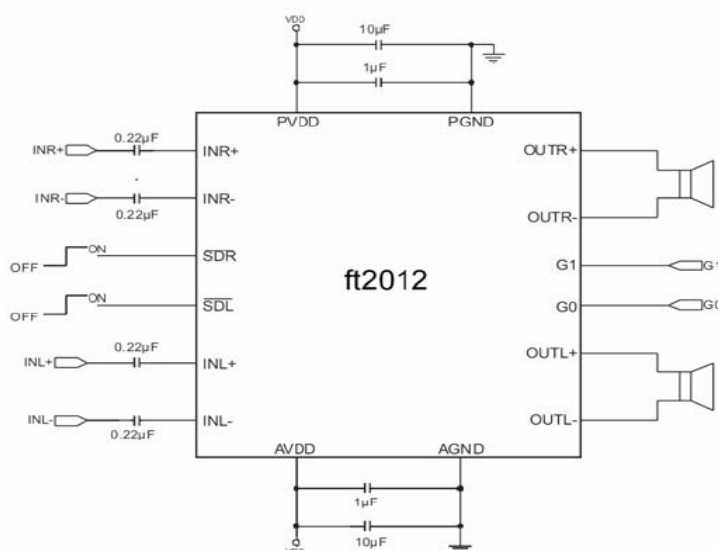
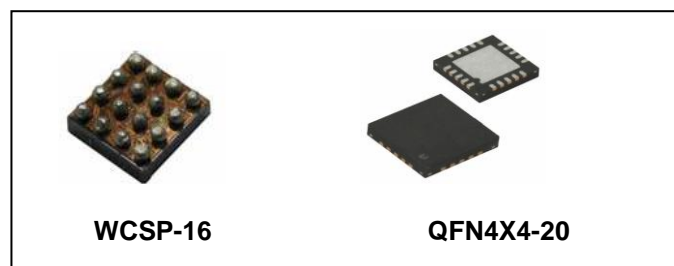


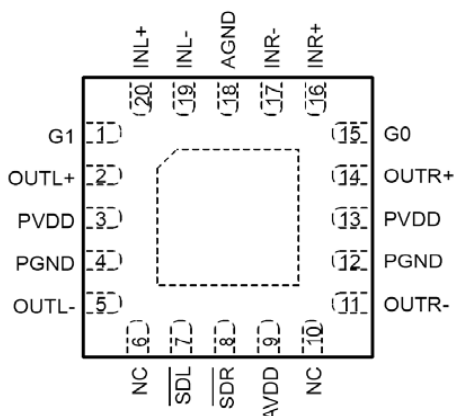
Figure 1: Typical Audio Amplifier Application Circuit

FEATURES

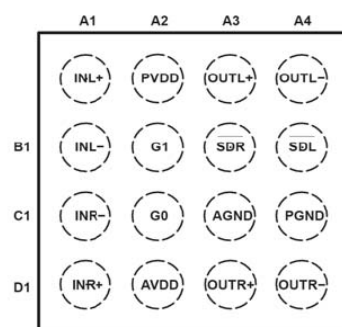
- Output Power at 5V
 - 2.8W/CH into 4Ω load at 10% THD
 - 1.65W/CH into 8Ω load at 10% THD
- High efficiency up to 90%
- High PSRR: 75dB (typical) at 217Hz
- Low THD+N: 0.10% at 1KHz (3.6V/8Ω/0.5W)
- Low quiescent current: 3.5mA at 3.6V with no load
- Shutdown current: 0.1μA (typical)
- Available in WCSP-16 and QFN4X4-20 packages



PIN CONFIGURATION AND DESCRIPTION



QFN 20 Top View



WCSP 16 Top View

NAME	QFN2X2-20	WCSP-16	I/O	DESCRIPTION
INR+	16	D1	I	Right channel positive input.
INR-	17	C1	I	Right channel negative input.
INL+	20	A1	I	Left channel positive input.
INL-	19	B1	I	Left channel negative input.
SDR	8	B3	I	Right channel active low shutdown control.
SDL	7	B4	I	Left channel active low shutdown control.
G0	15	C2	I	Gain select (LSB).
G1	1	B2	I	Gain select (MSB).
PVDD	3,13	A2	I	Power supply (must be same voltage as AVDD).
AVDD	9	D2	I	Analog supply (must be same voltage as PVDD).
PGND	4,12	C4	I	Power ground.
AGND	18	C3	I	Power ground.
OUTR+	14	D3	O	Right channel positive differential output.
OUTR-	11	D4	O	Right channel negative differential output.
OUTL+	2	A3	O	Left channel positive differential output.
OUTL-	5	A4	O	Left channel negative differential output.
NC	6,10	-	-	No internal connection.
Thermal Pad				Connect the thermal pad of QFN or WCSP package to PCB ground.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2012W	-40°C to +85°C	WCSP-16
ft2012Q	-40°C to +85°C	QFN4X4-20

FUNCTIONAL BLOCK DIAGRAM

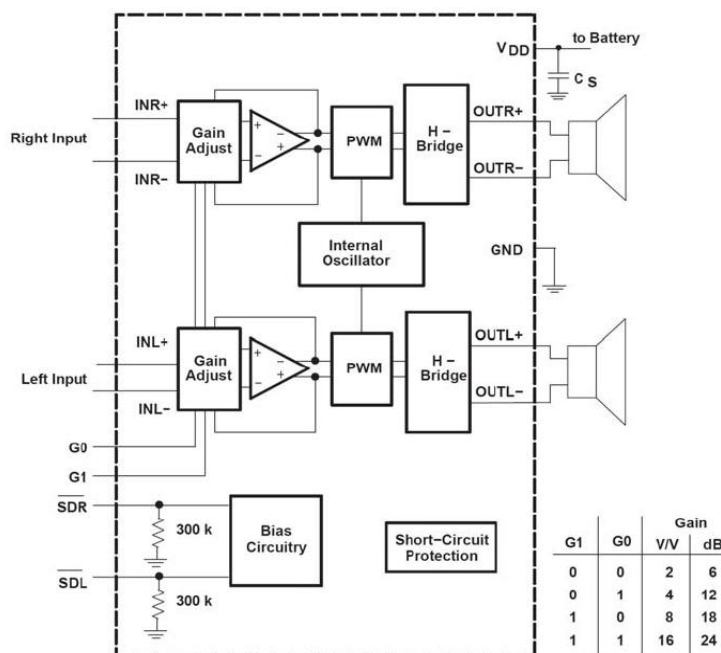


Figure 2: Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply voltage, VDD	-0.3V to 6.0 V
Input voltage (VI)	-0.3V to VDD+0.3V
Operating junction temperature range (TJ)	-40°C to 125°C
Operating free-air temperature range (TA)	-40°C to 85°C
Junction lead temperature(TL,Soldering,10s)	260°C
Storage temperature range	-65°C to 150°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	UNIT
WCSP-16	90 - 220	°C/W
QFN4X4-20	48	°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, VDD	2.7		5.5	V
High level input voltage, (VIH)	1.6		VDD	V
Low level input voltage, (VIL)	0		0.35	V
Operating temperature, TA	-40		+85	°C

ELECTRICAL CHARACTERISTICS

Note: The following electrical characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. But note that specifications are not guaranteed for parameters where no limit is given. The typical value however, is a good indication of device performance. All voltages in the following tables are specified at 25°C which is generally taken as parametric norm.

T_A=25°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage (measured differentially)	Inputs ac grounded, AV=6dB, V _{DD} =2.7V to 5.5V		5	25	mV
V _{UVLO}	Under-voltage lock-out threshold	V _{DD} falling		2.0		V
T _{OTP}	Over-temperature threshold			150		°C
	Over-temperature hysteresis			30		°C
PSRR	Power supply rejection ratio	V _{DD} =2.7V to 5.5V		75	55	dB
CMRR	Common mode rejection ratio	V _{DD} =2.7V to 5.5V		70	55	dB
I _{IH}	High-level input current	V _{DD} =5.5V, V _I =V _{DD}			50	μA
I _{IL}	Low-level input current	V _{DD} =5.5V, V _I =-0V			5	μA
I _{DD}	Supply current	V _{DD} =5.5V, no load or output filter		4.5		mA
		V _{DD} =3.6V, no load or output filter		3.5		
I _{SD}	Shutdown current			0.1		μA
r _{DS(ON)}	Static drain-source on-state resistance	V _{DD} =5.5V		420		mΩ
		V _{DD} =3.6V		520		
	Output impedance in shutdown mode	V _(SDR, SDL) =0V		2.5		KΩ
f _{SW}	Switching frequency	V _{DD} =2.7V to 5.5V		300		KHZ
	Closed-loop voltage gain	G1, G0=0V		6		dB
		G0= VDD, G1=0V		12		
		G0=0V, G1= VDD		18		
		G0, G1= VDD		24		

T_A=25°C, R_L=8Ω, A_v=6dB, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PO	Output power (per channel)	THD+N=10%, f=1KHz, R _L =4Ω	VDD=5V	2.8		W
		THD+N=10%, f=1KHz, R _L =8Ω	VDD=5V	1.65		W
			VDD=3.6V	0.85		
THD+N	Total harmonic distortion plus noise	VDD=5V, PO=1W, AV=6dB, f=1KHz, RC=8Ω		0.12		%
		VDD=3.6V, PO=0.5W, AV=6dB, f=1KHz, RC=8Ω		0.10		
PSRR	Power supply rejection ratio	VDD=5V, AV=6dB, f=217Hz		75		dB
		VDD=3.6V, AV=6dB, f=217Hz		70		

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V _n	Output voltage noise	VDD=5V, f=20 – 20KHz, Inputs ac-grounded, AV=6dB	No weighting		75		μVRMS
			A weighting		55		
	Channel crosstalk	VDD=3.6V, f=1KHz			-85		dB
CMRR	Common mode rejection ratio	VDD=3.6V, VIC=1Vpp	f=217Hz		-70		dB
SNR	Signal-to-noise ratio	VDD=5V, PO=1W, RL=8Ω			90		dB
Z _i	Input impedance	AV=6dB			28.1		KΩ
		AV=12dB			17.3		
		AV=18dB			9.8		
		AV=24dB			5.2		
	Start-up time from shutdown mode	VDD=3.6V			3.5		ms

Note: The ft2012 is thermally limited in WCSP and may not be able to deliver 2.8W/CH for 4Ω.

TEST SETUP FOR PERFORMANCE CHARACTERISTICS

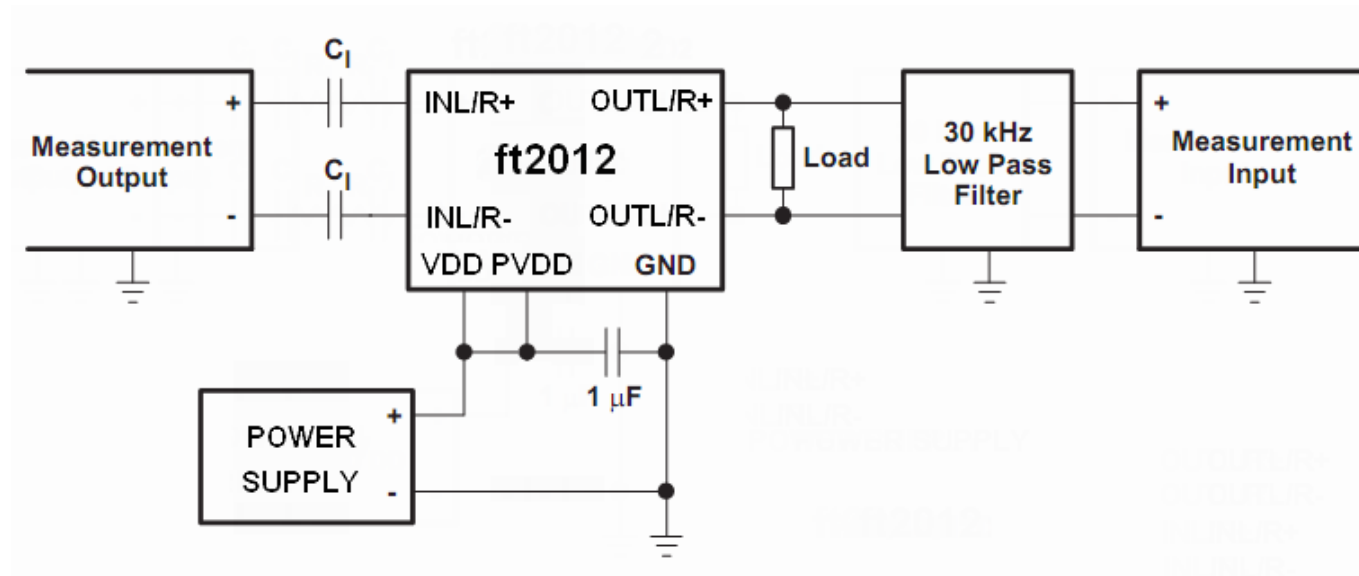


Figure 3: Test Block Diagram

Notes: (1) C_1 was shorted for any common-mode input voltage measurement; (2) A 33 μ H inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements; (3) The 30KHz lowpass filter is required even if the analyzer has an internal lowpass filter. An RC lowpass filter (100W, 47nF) issued on each output for the data sheet graphs.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $f = 1\text{KHz}$, $\text{Gain} = 6\text{dB}$, QFN-20 Package, unless otherwise noted.

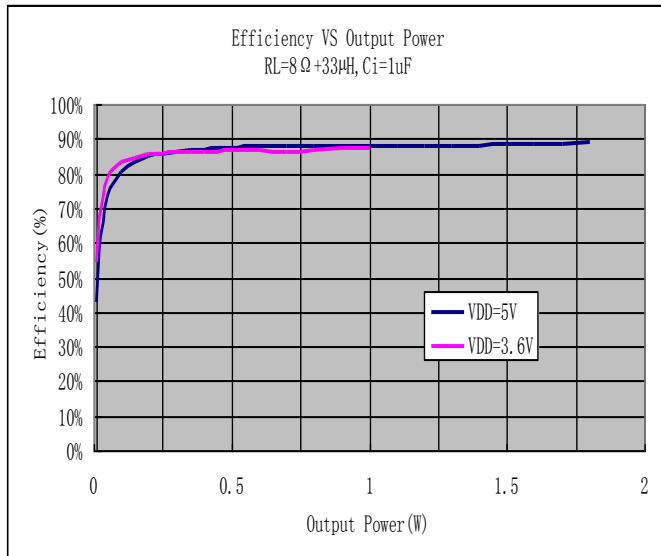


Figure 4: Efficiency vs. Output Power

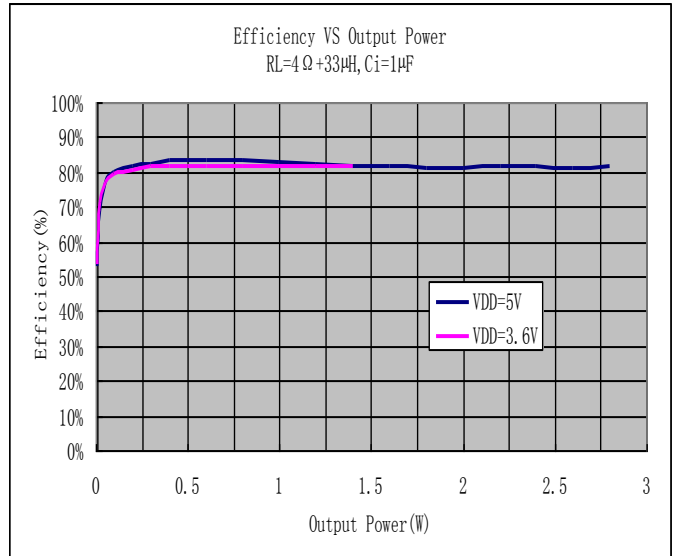


Figure 5: Efficiency vs. Output Power

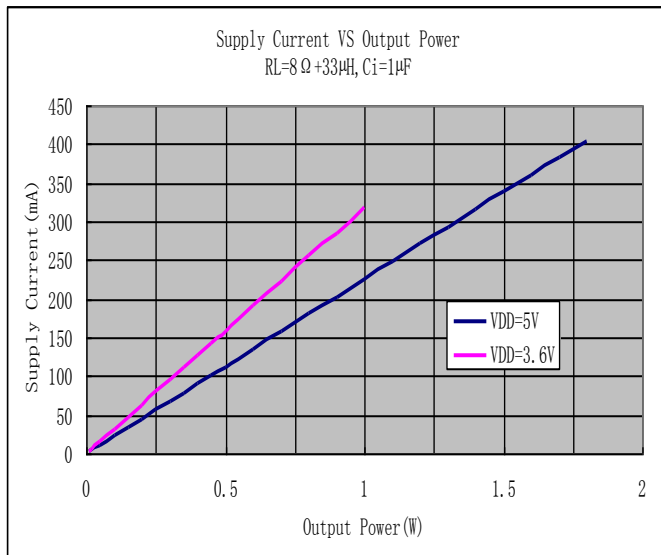


Figure 6: Supply Current vs. Output Power

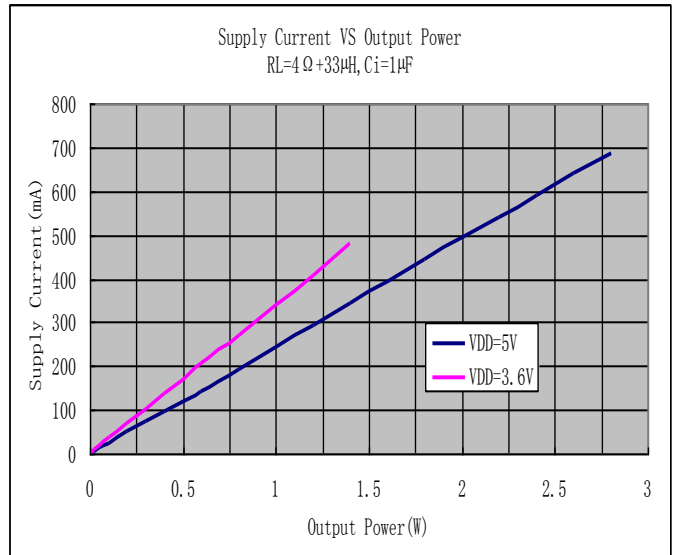


Figure 7: Supply Current vs. Output Power

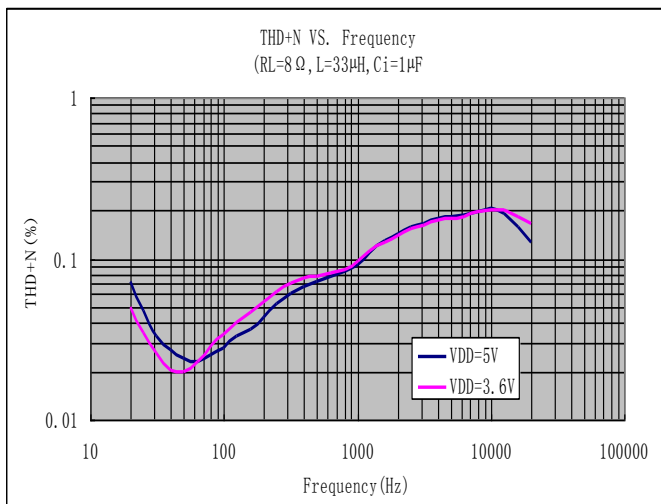


Figure 8: THD+N vs. Frequency

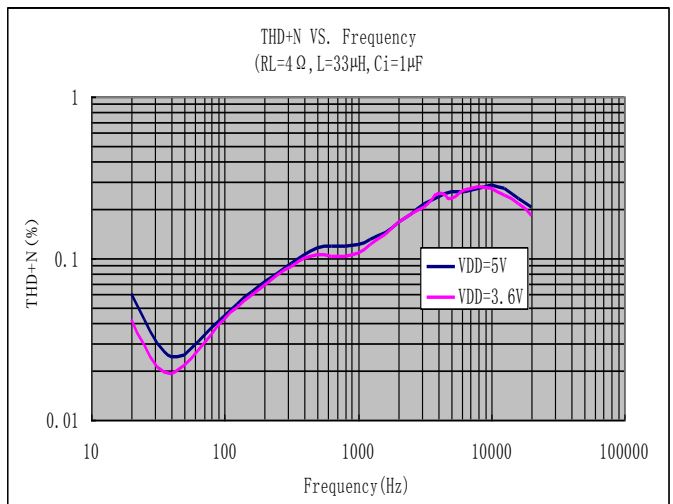


Figure 9: THD+N vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $f = 1\text{kHz}$, Gain=6dB, QFN-20 Package, unless otherwise notes.

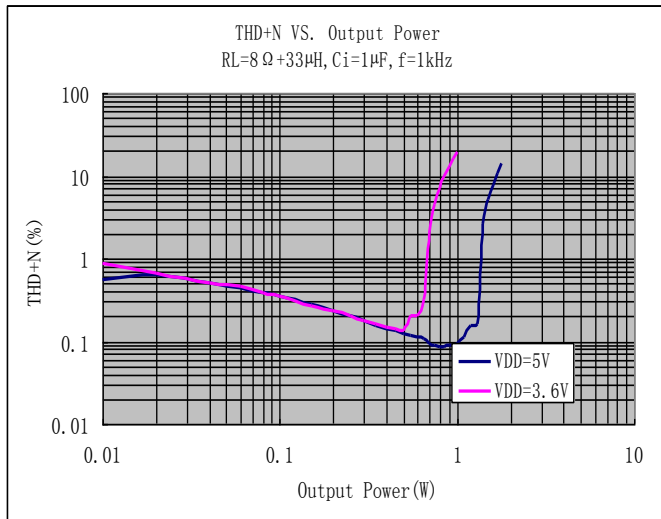


Figure 11: THD+N vs. Output Power

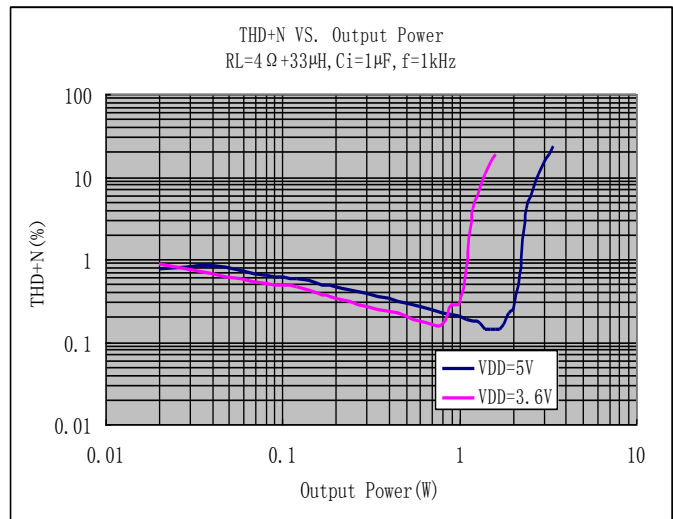


Figure 11: THD+N vs. Output Power

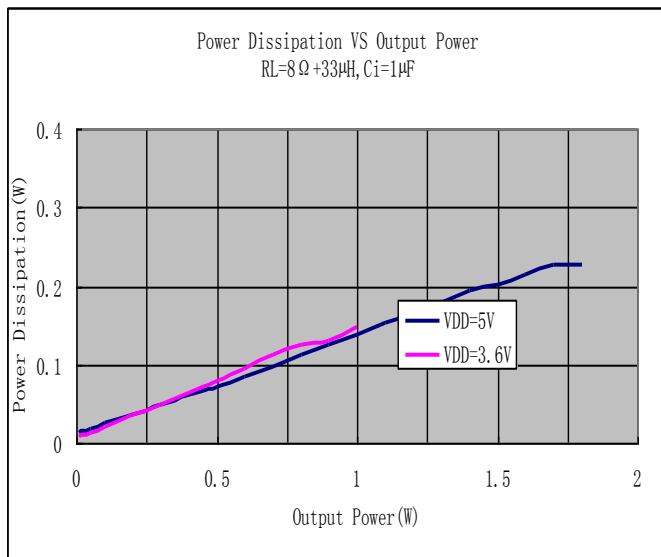


Figure 12: Power Dissipation vs. Output Power

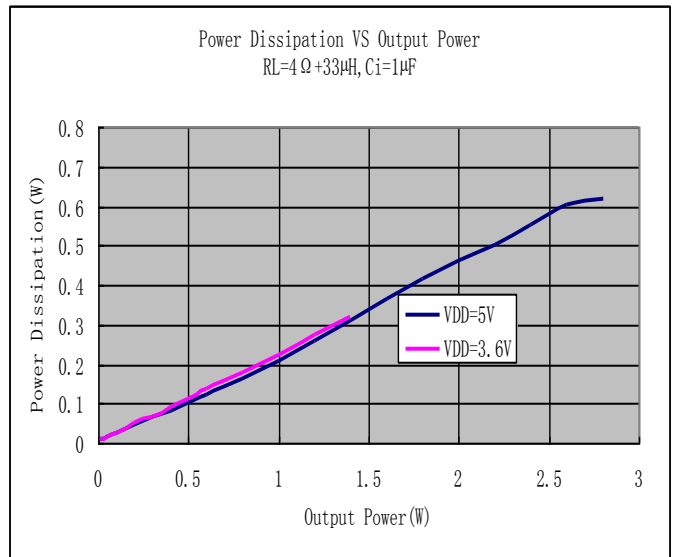


Figure 13: Power Dissipation vs. Output Power

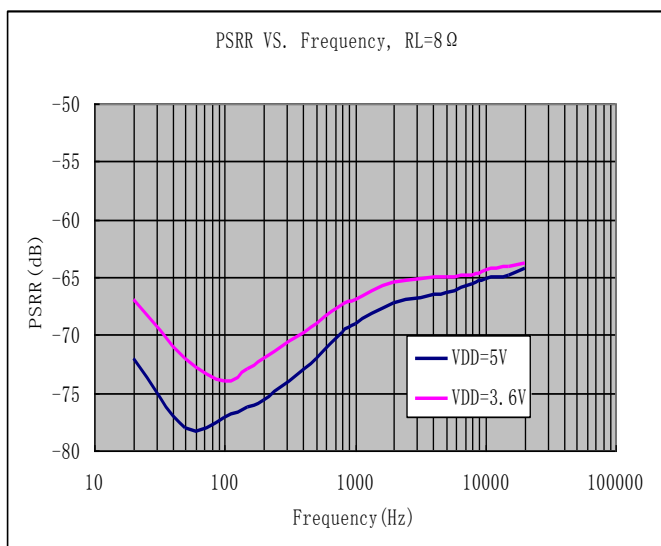


Figure 14: PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $f = 1\text{kHz}$, $\text{Gain} = 2\text{V/V}$, unless otherwise noted.

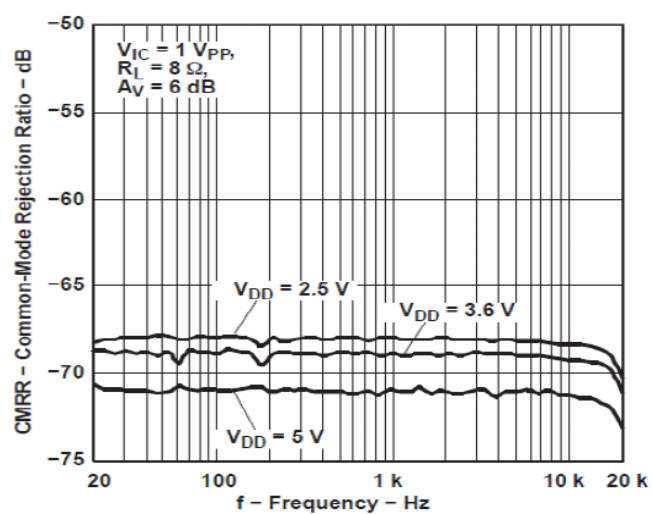


Figure 15: CMRR VS Frequency

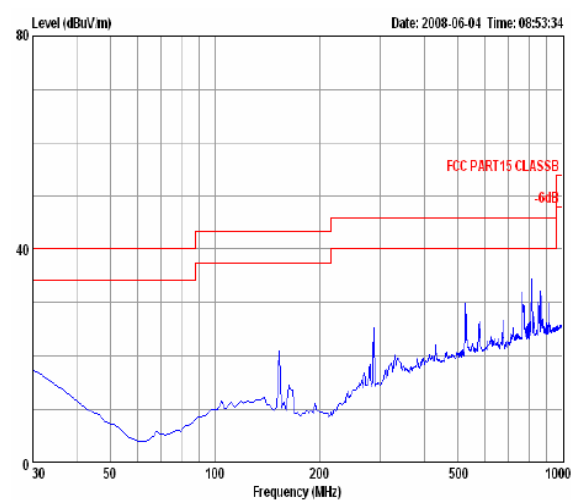


Figure 16: FCC Level

Fig

APPLICATION INFORMATION

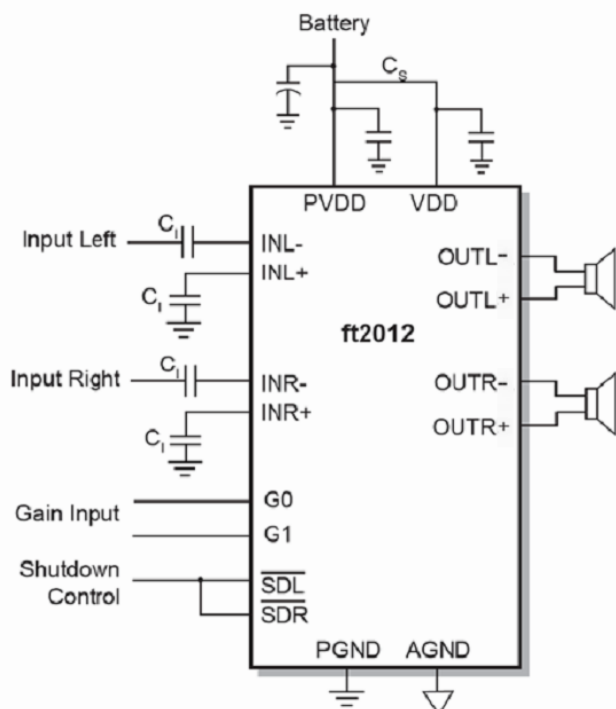


Figure 17: Application Circuit with Single-Ended Input

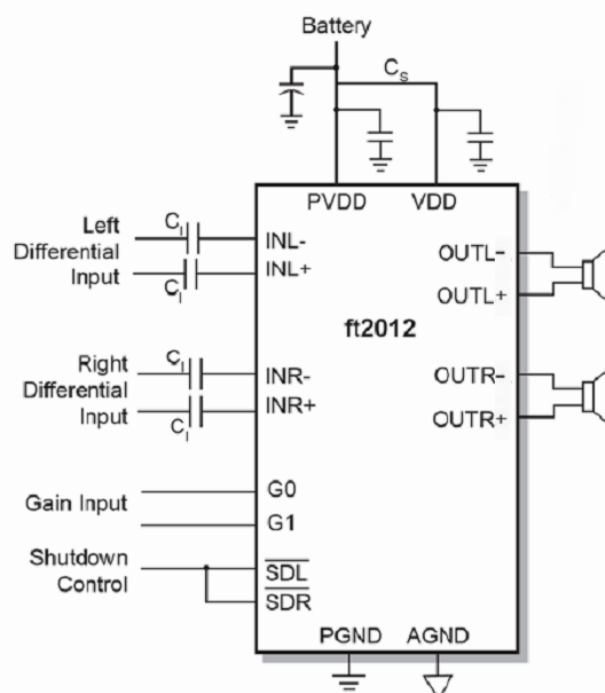


Figure 18: Application Circuit with Differential Input

DECOUPLING CAPACITOR (Cs)

The ft2012 is a high performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μ F, placed as close as possible to the device PVDD lead works best. Placing this decoupling capacitor close to the ft2012 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 μ F or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

AUDIO AMPLIFIER GAIN SETTING

The ft2012 features four internally configured gain settings. The device gain is selected through the two gain select pins, G0 and G1. The gain settings are shown in the following table.

Gain Setting Table

G1	G0	GAIN (V/V)	GAIN (DB)	RI (K Ω)
0	0	2	6	28.1
0	1	4	12	17.3
1	0	8	18	9.8
1	1	16	24	5.2

INPUT CAPACITORS (Ci)

The input capacitor and input resistor determine the corner frequency of the high pass filter. The corner frequency (fc) is calculated with the Equation (1) below.

$$f_c = \frac{1}{(2\pi R_i C_i)} \quad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation 2 is used to solve for the input coupling capacitance.

$$C_i = \frac{1}{(2\pi R_i f_c)} \quad (2)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

OPERATION WITH DAC AND CODEC

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (<1MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

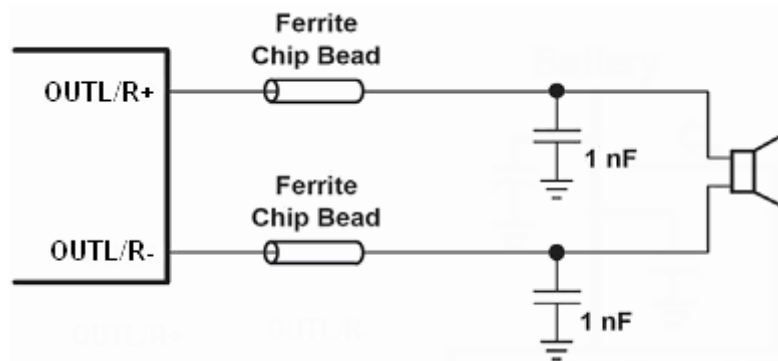


Figure 19: Typical Ferrite Chip Bead Filter

SHUTDOWN OPERATION ($\overline{\text{SDL}}/\overline{\text{SDR}}$)

In order to reduce power consumption while not in use, the ft2012 contains shutdown circuitry to turn off the amplifier's bias circuitry. It features independent shutdown controls for each channel.

This shutdown turns the amplifier off when logic low is placed on the $\overline{\text{SDL}}/\overline{\text{SDR}}$ pin. By switching the $\overline{\text{SDL}}/\overline{\text{SDR}}$ pin to GND, the ft2012 supply current draw will be minimized in idle mode.

UNDER VOLTAGE LOCK-OUT (UVLO)

The ft2012 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.0V or below, the ft2012 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or $\overline{\text{SDL}}/\overline{\text{SDR}}$ pin.

OVER TEMPERATURE PROTECTION

Thermal protection on the ft2012 prevents the device from damage when the internal die temperature exceeds 135°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

CLICK AND POP CIRCUITRY

The ft2012 contains circuitry to minimize turn-on and turn-off transients or "click and pops", where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 VDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

PCB LAYOUT

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the ft2012 and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the ft2012 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasitic capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and VDD in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the

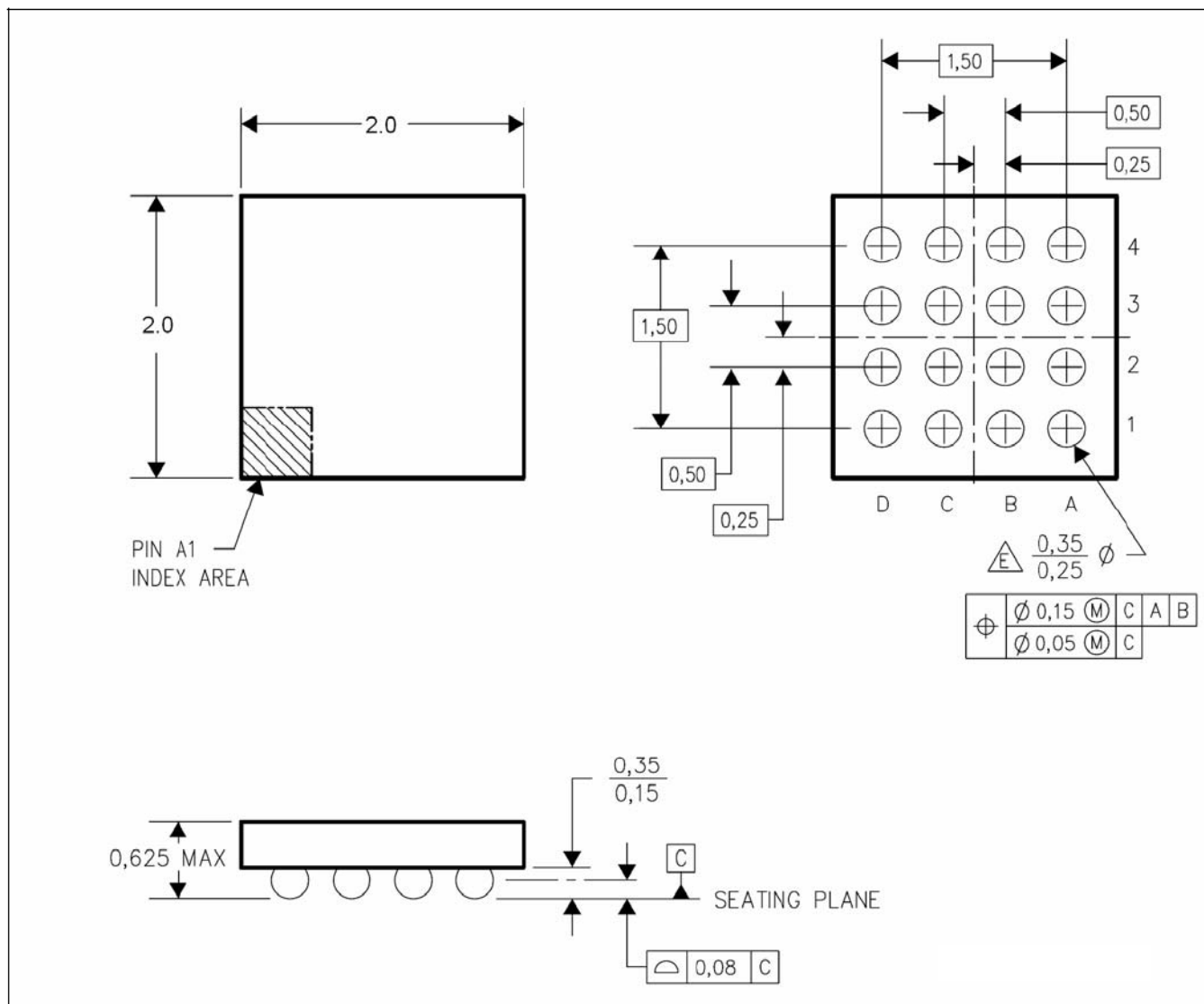
power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the ft2012 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite chip inductors placed close to the ft2012 may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

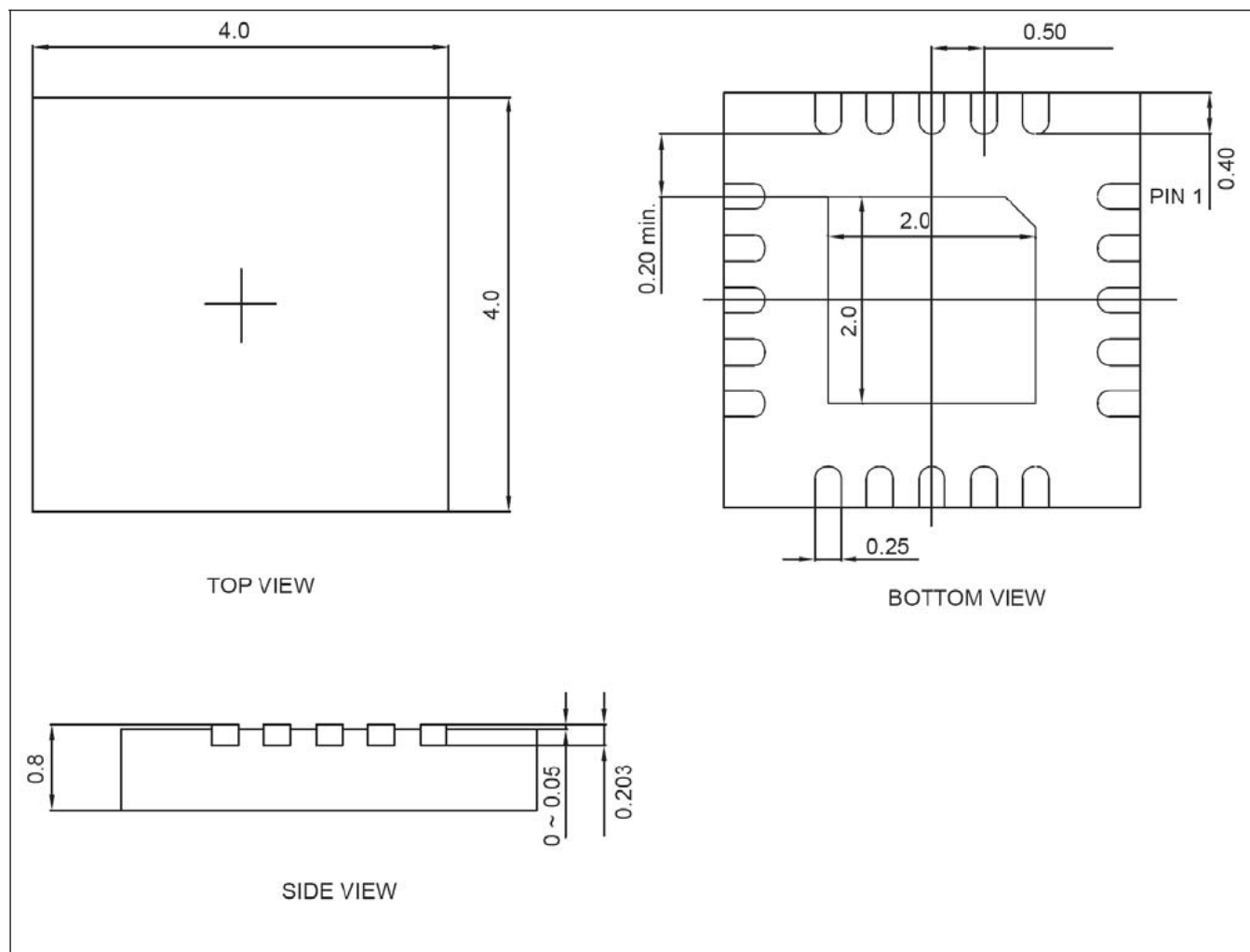
PHYSICAL DIMENSIONS

WCSP-16



Note: All Dimensions Are in Millimeters

QFN-20



Unit: millimeters.

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