

# ACECore MIL-STD-1553 Intellectual Property (IP) Core

MODEL: BU-69200



## FEATURES

- Modular and Universally Synthesizable Code for Enhanced Mini-ACE
  - Industry Standard, Proven Design
  - Use Enhanced Mini-ACE Hybrid for Prototyping
- Includes VHDL Design and VHDL Test Bench Code
- BC/RT/Monitor and RT-Only Configurations.
- Single Clock Domain, Selectable for 10, 12, 16, or 20 MHz Operation
- Fully Synchronous Design
- Approximately 20,000 ASIC Gates for BC/RT/MT Instantiation, Highly Optimized Design
- Provision for up to 64K Words Off-Core Buffer RAM, with Optional RAM Parity Bit
- Provision for Off-Core Built-In Self-Test ROM
- On-Core Buses are Unidirectional (not tri-state). Tri-State Buses May be Created Using Off-Core Buffers
- Instantiate on FPGAs or ASICs
- Passed MIL-STD-1553 RT Validation Testing
- Compatible with DDC Transceivers
- Complete Documentation Provided
- Scalable to Higher Bit Rates
- Applications:
  - Space/Rad Hard Applications
  - High Volume Applications

## DESCRIPTION

The ACECore Intellectual Property (IP) is based on the architecture of DDC's powerful Enhanced Mini-ACE MIL-STD-1553 protocol engine. As such, it provides compatibility with all previous and current generations of DDC components, including AIM-HY, AIM-HY'er, ACE, Mini-ACE, as well as Enhanced Mini-ACE, PCI Enhanced Mini-ACE, and  $\mu$ -ACE.

As a result, the ACECore IP brings a legacy of demonstrated performance in a myriad of air, land, and space applications. Further, this compatibility enables designers to leverage investments in legacy ACE software and to accelerate development efforts using DDC's components early in their design phase.

The ACECore provides VHDL core source code, VHDL test bench, and supporting documentation, thus enabling designers to instantiate the architecture in a variety of PLD, FPGA, or ASIC System on a Chip (SoC) implementations.

The ACECore can be configured as BC/RT/MT, RT-only, or customized for your requirements. The core provides a high degree of flexibility in terms of processor interface, memory architecture, and self-test functionality. To minimize design risk, the design of the ACECore's manchester encoder/decoder is highly optimized for use with DDC's 5V or 3.3V transceivers.

The ACECore's advanced bus controller architecture provides methods to control message scheduling, along with the means to minimize host overhead for asynchronous message insertion, facilitate bulk data transfers and double buffering, and support various message retry and bus switching strategies.

The ACECore's remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. The choice of RT data buffering and interrupt options provides robust support for synchronous and asynchronous messaging, while ensuring data sample consistency and supporting bulk data transfers. The ACECore message monitor (and combined RT/Monitor) enables true message monitoring, with filtering on an RT address/T-R bit/sub-address basis. The ACECore includes provides robust built-in self-tests for protocol, transceivers, and RAM.

## Specifications

PARAMETER	MIN	TYP	MAX	UNITS	PARAMETER	MIN	TYP	MAX	UNITS
<b>ASIC GATE COUNT</b>		20,000			<b>1553 MESSAGE TIMING</b>				
<b>CORE CONFIGURATIONS</b>	BC/RT/Monitor, RT-only				BC Intermesssage Gap		9.5		μS
<b>PROTOCOLS SUPPORTED</b>	MIL-STD-1553A/B Notice 2 STANAG-3838 MIL-STD-1760				- Non-enhanced (Mini-ACE compatible) BC mode - Enhanced BC Mode		10.0 to 10.5		μS
<b>MEMORY SUPPORT</b>					BC/RT/MT Response Timeout				
1553 Message, Control, and Status RAM	64K X 16 or 64K X 17				18.5 nominal	17.5	18.5	91.5	μS
Protocol Self-Test ROM or RAM	4K X 24				22.5 nominal	21.5	22.5	23.5	μS
					50.5 nominal	49.5	50.5	51.5	μS
					128.0 nominal	127	129.5	131	μS
<b>CLOCK INPUT</b>					RT Response Time (mid-parity to mid-sync)	4		7	μS
Number Of Clock Domains	1				Transmitter Watchdog Timeout		660.5		μS
Frequency: Nominal Values					<b>SOURCE CODE LANGUAGE</b>	VHDL			
Default Mode		16.0		MHz	<b>SUPPORT DOCUMENTATION</b>	ACECore IP User's Guide Enhanced Mini-ACE User's Guide			
Option		12.0		MHz					
Option		10.0		MHz					
Option		20.0		MHz					

### BC Architecture

- Highly Autonomous Message Sequence Control
- Defined Set of 20 Instructions
- Control/Status Blocks for Individual Messages
- Minor and Major Frame Scheduling
- Asynchronous Message Insertion
- Conditional Branching and Subroutines
- General Purpose Queue: Message Status, Time, Immediate and Indirect Data
- Fully User-definable Interrupts
- Legacy Mode for Compatibility with ACE and Mini-ACE Applications

### RT Architecture

- Supports MIL-STD-1553A/B Notice 2, STANAG-3838 RT, and MIL-STD-1760 Stores Management
- Choice of Subaddress Single Message, Double Buffering, or Circular Buffering; or Global Circular Buffering
- 32-Entry Interrupt Status Queue
- 50% and 100% Circular Buffer Rollover Interrupts
- Stack with Descriptors for Individual Messages
- Message Status, Time Tag, Command Word, Data Pointer

- Programmable Command Illegalization
- Programmable Busy by Subaddress
- Interrupts on All Messages, or Individual Subaddresses and/or Mode Codes
- Hardwired or Software-Programmable RT Address
- Available with Option for RT AUTO-BOOT with BUSY Bit Set for MIL-STD-1760 Applications
- Compatible with ACE and Mini-ACE Applications

### Monitor Architecture

- Selective Message Monitor
- Filter Based on RT Address, T/R\* bit, Subaddress
- True Message Monitor
- Command Stack
- Message Status, Time Tag, Command Word, Data Pointer
- Data Stack
- All Monitored Words Following (first) Command Word
- 50% and 100% Rollover Interrupts for Command and Data Stacks
- 32-Entry Interrupt Status Queue
- Simultaneous RT/Message Monitor Option

### Autonomous Built-In Self-Test Capability

- Protocol Self-Test
- RAM Self-Test
- Online Loopback Test
- Capability to Support Channel A-to-Channel B Wraparound Test
- Capability to Test Transmitter Timeout Function
- Protocol Self-Test May be Run From External Host

### Host and Memory Interface Configurations

- Shared RAM, Up to 64K X 16 or 64K X 17 (with RAM parity)
- 16-bit Address, 16-bit or 8-bit Data Path
- "Zero Wait State" Interface (no hardware acknowledge) for Microcontrollers
- Support of DMA Configuration, Enabling Core Access of RAM on Host Processor Bus
- Supports Use of External Dual Port RAM

### Development Environment/Tools

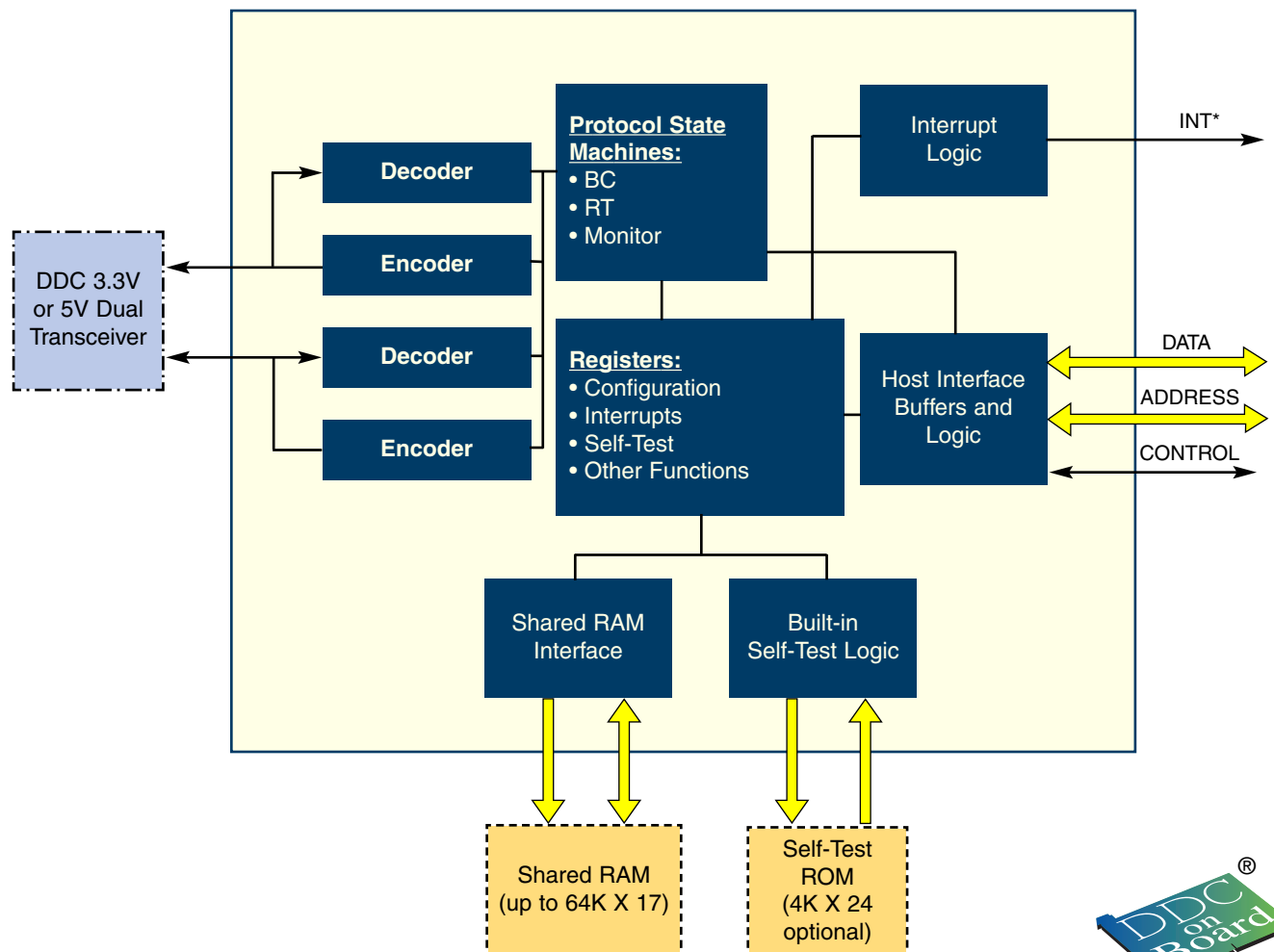
- DDC Development Tools: Mentor Graphics Workstation; Renoir Design Entry (Including for Block Diagrams); Leonardo Synthesizer; Model Technology Simulation Tool
- Sample Synthesis Scripts
- VHDL Test Bench

### Miscellaneous

- Reset Philosophy: Hardware and Software Mechanisms for Resetting All Flip-Flops
- No On-Chip Tri-State Buses.

## ACECore Functional Blocks

Figure 1



**BU-69200 X X**

**Base Product**

BU-69200 = MIL-STD-1553 ACECore Intellectual Property

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## Architecturally Compatible Products

- AIM
- AIM HIGHER
- ACE
- Mini-ACE™
- Enhanced Mini-ACE™
- m-ACE™ (Micro-ACE) Series
- Mini-ACE™ Mark3 Series

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